Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.017”**

**.017”**

**BASE**

**EMITTER**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003” X .003”**

**Backside Potential: COLLECTOR**

**Mask Ref: G36**

**APPROVED BY: DK DIE SIZE .017” X .017” DATE: 9/7/21**

**MFG: ZETEX THICKNESS .005” P/N: 2N918**

**DG 10.1.2**

#### Rev B, 7/19/02